A Highly Integrated GPS Receiver for Cellular Handset

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***Abstract* — A highly integrated dual conversion heterodyne GPS receiver is reported. The receiver chip includes a 2.9dB NF LNA, an image-reject mixer with 32dB image rejection. The on-chip IF chain, which consists of a VGA, a 2nd mixer and filtering, has a maximum gain of 83dB, a gain range of 45dB and a 7dB NF. A 4-bit ADC is integrated on chip for enhanced SNR. The PLL with its VCO are also integrated. The total NF is 3dB with a total 121dB voltage gain. The chip consumes 132mW at 2.7V.**

I. Introduction

Many commercial GPS systems are currently available for a variety of applications such as automotive, recreational, etc. They use the L1 band, centered at 1575.42 GHz, which carries the C/A code. The recent FCC requirement, for an Enhanced 911(E911) system for locating wireless callers, has raised the level of interest in GPS receivers. Such receivers must be integrated within the handset, and must operate in the presence of interferers originating from the transmitters within the handset device. They must also consume low power. All these requirements make GPS receivers, for handsets, more challenging to design than those intended for other applications.

Several GPS receiver implementations have been reported recently [1-3]. A very low power implementation, reported in [1], uses a large number of external components. It uses an off-chip LNA (active antenna), external SAW filters and an external tank for the VCO. Another realization [2], which is claimed to be highly integrated solution, uses two chips; a GaAs RF chip and a CMOS IF/analog chip. The 0.5μm bipolar implementation of a GPS receiver in [3] has a high integration level. It uses three off-chip filters and includes a 2 bit ADC.

The GPS receiver reported, here, is designed to operate in GSM and CDMA IS95 phones. The frequency plan was designed to accommodate the interferers generated by the transmitters for both standards. The level of integration is the most aggressive to date. The receiver is implemented in a low-cost 0.6μm BiCMOS process.

II. Receiver GPS Architecture

The block diagram of the receiver is shown in Fig. 1. The receiver architecture is a highly integrated dual conversion heterodyne, chosen for its robustness and flexibility. All the circuitry is differential to reduce substrate noise injection and coupling, which is an important consideration because of the very high total voltage gain. The single-ended input signal is amplified and immediately converted to differential by a single stage LNA, which drives an image rejection mixer (IRM). In a stand-alone GPS application the image rejection from the preselector filter is often sufficient, so no extra rejection is needed for the image. But because this chip was designed for wireless phone applications, where extra spurs could be present at the image frequency, it is necessary to provide some attenuation at those frequencies.

The signal is filtered, externally, at the first IF and then amplified by an AGC and downcoverted to the second IF by the 2nd mixer. The AGC is employed to compensate for the overall chain gain variation over process and temperature. It was also designed to handle the in-band jammers to avoid saturating the ADC. After the second mixer, the signal is filtered by a 3rd order integrated Gm-C filter. The filter is followed by a fixed gain amplifier, which drives a 4 bit ADC. The ADC output signal has CMOS compatible digital levels.

All local oscillator signals are generated internally by a programmable integer synthesizer, which includes: a VCO with integrated LC tank, prescaler, phase/frequency detector and charge pump.

III. Receiver Implementation

A. LNA and Image Reject Mixer

A single stage single-ended to differential LNA has been implemented. A fully differential structure would have been preferred, because of its immunity to substrate noise coupling. However, differential LNAs need one extra input pin and more external components for a single-ended to differential transformation.

Particular care was used in the pin-out and layout of this block to minimize noise and spurious coupling

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through the substrate and the package. To improve the linearity (i.e. the maximum output voltage swing) and reduce the NF two on-chip inductors have been used as loads for the LNA (Fig. 2). The LNA and the Mixer are AC-coupled through two series capacitors, used also as matching components, in order to maximize the power transfer between the two blocks and reduce the noise contribution from the mixer.

Two different image-reject mixer (IRM) architectures were investigated. The first uses the conventional polyphase filter for generating the quadrature local-oscillator (LO) signals [see Fig. 2(a)]. A 2-stage polyphase filter was found to be sufficient to generate LO signals with less than 1 degree phase error. The 2nd stage is needed, mainly, to equalize the amplitudes of in- and quadrature- phase signals. Using a single-stage polyphase causes significant imbalances in these signals, mainly due to the process variations of the resistors and capacitors.

In the 2nd architecture [see Fig. 2(b)], the voltage-controlled oscillator (VCO) operates at twice the LO frequency (2.7 GHz) and dividers were used to generate the quadrature LO. After due evaluation, the 2nd architecture was chosen, because of the power savings it offered.

After the 2 mixers, another polyphase filter is used to attenuate the image. Again, a 2nd order network was used to provide adequate image rejection. Since no tuning was used, the polyphase filter was designed to have adequate bandwidth so that image rejection remains immune to the process variations of resistors and capacitors.

B. IF Chain

The IF chain consists of four major blocks before the signal is digitized by the ADC as shown in Fig. 1. The first block is a VGA with discrete 3 dB gain steps. The total gain range is 45 dB. The selection of gain is controlled by a digital AGC loop. The input to the digital AGC comes, directly, from the ADC output. The signal power is measured through an absolute-value block. The integration and threshold control is then computed to control the VGA. The 4-bit ADC gives a large window for the threshold of the input noise [4]. The 45 dB gain range, of the VGA, was chosen based on the in-band jamming specifications. The highest level of co-channel jamming designed for was 30 dB above the thermal noise floor. A signal off channel will be rejected by the RF preselect filter, in front of the LNA, and additional filtering by the SAW filter after the first mixer and LPF after the second mixer.

The next block is a standard double balanced mixer. The output is directly fed into a 3rd order Gm-C LPF. The cut-off frequency of the filter is tuned, upon chip enabling, to account for process variations. The tuning is achieved by adjusting the biasing current of the Gm cells using a DAC. The tuning scheme is based on a master-slave approach. A Gm-C oscillator, which uses Gm cells identical to those used in the filter, is turned on during power-up. During the tuning process, the biasing current of all Gm cells is varied until the frequency of the oscillator is tuned to a fixed reference frequency. This will guarantee that the cut-off frequency of the filter is also tuned to the desired value. The routine used is based on a successive approximation technique. The MSB of the DAC is first determined then each successive bit is set. Fig. 3 shows the typical filter frequency response after tuning. The final block, in the IF chain, is an amplifier used to provided the ADC with the correct noise level. The gain is based on resistor matching using standard op-amp techniques. The output driver is a low impedance stage to drive the ADC

C. VCO and PLL

A single PLL is used to synthesize the needed frequencies as shown in Fig. 1. A conventional PLL architecture was fully integrated on chip except for the loop filter, which requires a large capacitance.

The VCO oscillates at double the LO frequency. This is divided by a master slave flip-flop to generate the I and Q components of LO. The VCO is an LC tuned oscillator with parallel negative resistance. The LC tank resonator is completely integrated using an on-chip Schottky-diode varactor and bondwire inductance. The Schottky-diode varactor offers a good Q (above 15) in the 2GHz range when the signal is applied on the anode of the diode (the Schottky contact). If the signal is on the cathode (NWELL side) the Q is very poor due to losses in the NWELL/p-substrate junction. In addition, the large NWELL/p-substrate capacitance reduces the tuning range of the diode. Two cross-coupled PMOS devices are used to realize the negative resistance.

The tank inductances were realized using the bond wire between the pad and the package pin. A package model was employed to estimate this inductance. The inductance available was 1nH. Bondwires provide very high Q inductances. The mutual inductances due to the neighboring bondwires have been matched. Since the control over the die mounting and bonding is quite precise, the variation in the bondwire inductance is very small. This variation as well as the variation of the capacitances of the PMOS gate, the pn junctions and the varactors, due to process and temperature, has to be covered by the tuning range of the varactors. Since in

GPS only one LO frequency is needed, the tuning range available from the varactors was enough.

An amplitude control loop was employed to set the oscillation amplitude at a desired level. The output of the amplitude control loop controls the DC bias at the gate of the PMOS devices. The common-mode source degeneration resistance is used to set the gain of the amplitude control loop for stability purpose. This resistance also helps to attenuate the phase noise contribution of the amplitude control loop.

D. ADC

The quantization error of the ADC impacts the SNR of the GPS receiver. Increasing the number of bits reduces the SNR degradation. According to [5], 4-bit resolution provides close to minimum SNR degradation. Going to higher resolution offers very little improvement. A 4-bit ADC is, therefore, a good compromise between SNR degradation and complexity.

A 4-bit ADC was integrated on the chip. The sampling rate is 20MHz. A flash architecture seemed most suitable. It achieves the desired sampling rate with reasonable current consumption. The ADC consists of a resistive ladder, 15 preamplifier/comparator cells, bubble logic, the encoder, CMOS-level output buffers and the biasing. A CMOS switched-capacitor fully differential structure was chosen for the preamplifier/comparator cell. Special care was needed to minimize the offset, which is critical for some baseband algorithms such as SnapTrack.

III. Measurements and Results

The receiver was implemented in a 0.6μm BiCMOS process. The die area is 25mm^2. The total power consumption is 132mW at 2.7V supply. Table I summarizes the typical key performance parameters. Fig. 4 shows the phase noise of the VCO at RT and 85°C. The phase noise improves at cold temperature. The whole receiver was tested using a single tone at the input. Fig. 5 shows the resulting measured spectrum at the output.

IV. Conclusion

A highly integrated GPS receiver implementation was presented. An external image-reject SAW filter is not needed because of the IRM implementation. The integrated LC tank of the VCO saves a number of external components as well. Finally, the 4-bit ADC offers improved SNR and makes the receiver compatible with Snap Track baseband. With a slight modification to the frequency plan, this receiver can be used for other baseband solutions.

References

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TABLE I
SUMMARY OF MEASURED PERFORMANCE

LNA + IRM		
Gain		32 dB
NF		2.9 dB
P 1dB		-33 dB
Image Rejection		32 dB
IF Chain		
Max Voltage Gain		83 dB
NF @ max gain		7 dB
Input 1dB Comp. @max gain		-84 dBVrms
Voltage Gain Range		45 dB
Gain Error (linearity)		+/-1 dB
3 dB Corner Frequency		4 MHz
ADC		
DNL		+/-0.15 LSB
INL		+/-0.15 LSB
Differential Offset		+/- 0.1 LSB
ENOB		3.9
SNR		26.5 dB
SINAD		25.5 dB
THD		-31 dBc
VCO and PLL		
Phase noise of free run. VCO at 1359 MHz	10 kHz	-80 dBc/Hz
	100 kHz	-101 dBc/Hz
	1 MHz	-120 dBc/Hz
	5 MHz	-125 dBc/Hz
RMS Phase Error		5 degrees
Lock Time		1.2 msec
Total Chip		
Voltage Gain		121 dB
NF		3 dB

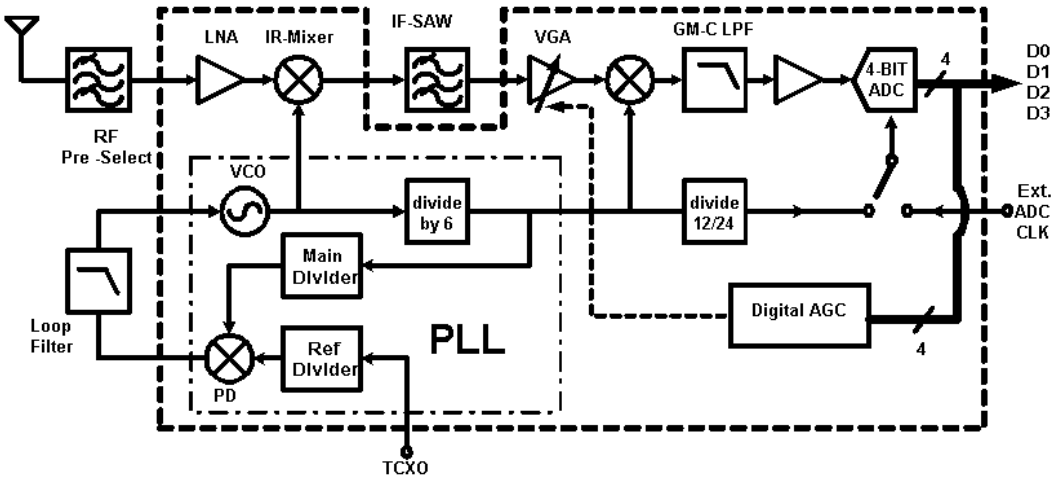

Fig. 1. The architecture of the GPS receiver. The dashed box defines the chip boundaries

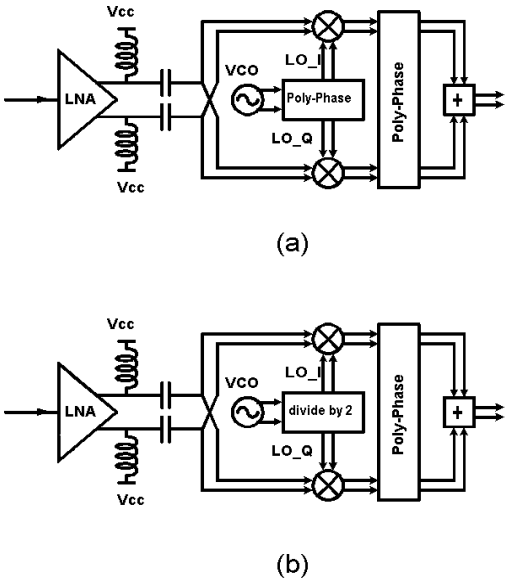

Fig. 2. LNA and IMR topologies

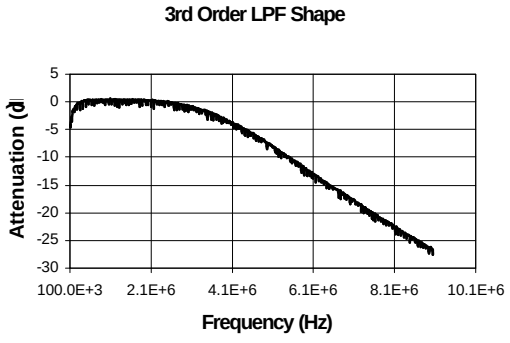

Fig. 3. Third order low pass filter shape after tuning.

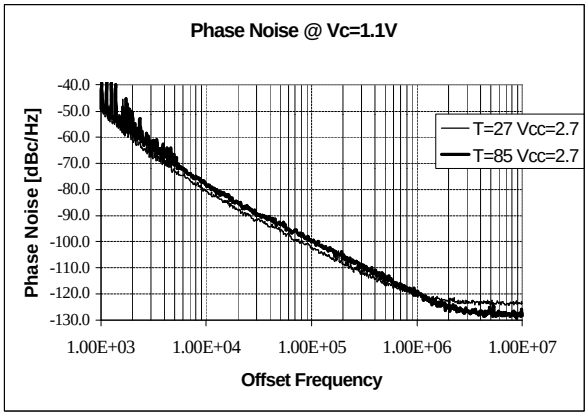

Fig. 4. The phase noise of the VCO for RT and 85°C.

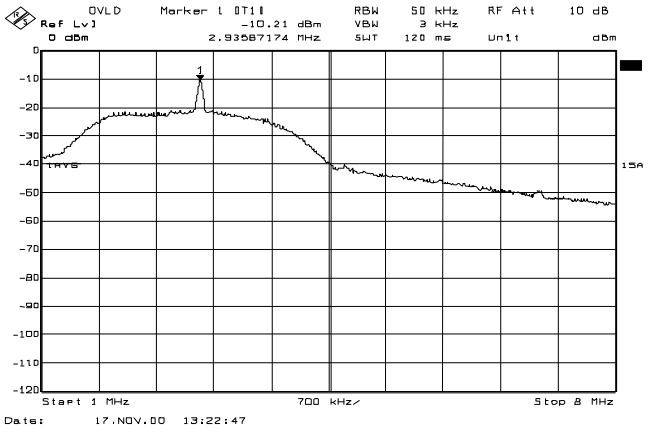

Fig. 5. The spectrum at the receiver output with a single tone at the input.